AMENDMENTS TO THE SPECIFICATION:

Please replace the paragraph [0004] beginning at page 2, line 23, with the following rewritten paragraph:

[0004] In accordance with system on chip (SOC) technology, a variety of circuit building blocks are incorporated onto a single integrated chip. Each of the building blocks performs a specific function of an electronic system. The IP building blocks include, but are not limited to, embedded memory, standard cell, I/O devices, analog and system interfaces, ~~etc....~~ etc.

Please replace the paragraph [0022] beginning at page 5, line 14, with the following rewritten paragraph:

[0022] Referring now to the drawings wherein the showings are for purposes of illustrating preferred embodiments of the present invention only, and not for purposes of limiting the same, Figure 1 is a flowchart illustrating an automatic method of identifying sense amplifier inputs and verifying the sensed bit-bitb voltage difference against a noise margin in memory designs. Referring to Figure 2, a sense amplifier 10 having a bit line 12 and a bitb line 14 is shown. Figure 3 shows a graph illustrating a comparison of voltage differences between the bit 12 and bitb line 14 for the sense amplifier 10 shown in Figure 2. The sense amplifier 10 is a basic building block used in the design of memory circuits. A sense amplifier enable (SAE) line 16 is also an input to the sense amplifier 10 and controls the time when the voltage on the bit line 12 and the bitb line 14 are sensed. If the voltage difference between the bit line 12 and the bitb line 14 at sensing time (as controlled by the SAE line 16) is

less than the noise margin for the signals, then the reliability of the signals can be in question. Therefore, it is advantageous to verify the sensed bit-bitb voltage against the noise margin in memory designs.

Please replace the paragraph [0029] beginning at page 8, line 20, with the following rewritten paragraph:

[0029] In step 213, a current OP is determined to be the average of the current minimum OP and the current maximum OP. In step 207, it is determined whether there is convergence within the circuit. Specifically, convergence is based upon whether the current CP is within a specified error tolerance. If convergence is reached, then in step 208, the current OP is the minimum clock and the process stops. However, if convergence is not reached, then the circuit is simulated with the current OP and the CP, DO_Err and current SSAI is calculated in step 209. In step [[201]] 210, it is determined whether the simulations have succeeded in the same manner as step 205. If the simulations have succeeded then the process continues to step 211 where the current OP is the minimum OP and the process returns to point "A" for iterative bisection. However, if the simulations fail, then in step 212, the current OP is set as the maximum OP and the process proceeds to point "A" for iterative bisection. As will be recognized by those of ordinary skill in the art, at point "A", the process will continue until there is convergence in step 207.